NATIONAL INSTITUTE OF TECHNOLOGY SILCHAR

Syllabus

M. Tech

Microelectronics & VLSI Design (MVD)

Department of Electronics & Communication Engineering
Curriculum and Syllabi for M. Tech. in Microelectronics & VLSI Design (MVD)
With effect from 2019 entry batch

PO Statements:

1. An ability to independently carry out research /investigation and development work to solve practical problems.
2. An ability to write and present a substantial technical report/document.
3. Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program
4. An ability to understand and design advanced VLSI-based systems and conduct experiments, analyze and interpret results.
5. To use the techniques, skills, modern electronic design automation tools, software, and equipment necessary to evaluate and analyze the systems in VLSI design environments.
6. Graduates will be able to plan, conduct an organized and systematic study on significant research topic within the field of VLSI and its allied field.

Course Structure

Semester I

S. N.	Code	Subject	L	T	P	Credits
1.	EC 5201	Semiconductor Device Physics	3	0	0	3
2.	EC 5202	Digital VLSI Design	3	0	0	3
3	EC 5203	Device Modelling	3	0	0	3
4.	EC 5204	VLSI Lab I	0	0	3	2
5.	EC 5210	Seminar	0	0	2	1
6.	EC 52xx	Elective I	3	0	0	3
7.	EC 52xx	Elective II	3	0	0	3
		Total contact hours/credits	15	0	5	18

Semester II

S. N.	Code	Subject	L	T	P	Credits
1.	EC 5211	Analog VLSI Design	3	0	0	3
2.	EC 5212	VLSI System Testing & Verification	3	0	0	3
3	EC 5213	VLSI Technology	3	0	0	3
4.	EC 52xx	Elective III	3	0	0	3
5.	EC 52xx	Elective IV	3	0	0	3
6.	EC 5214	VLSI Lab II	0	0	3	2
7.	EC 5220	Colloquium	0	0	2	1
8.	EAA	Extra Academic Activities (Yoga)	0	0	2	0
		Total contact hours/credits	15	0	7	18

Semester: III and IV

S. N.	Code	Subject	L	T	P	Credits	Semester
1	EC 6298	Project phase-I	-	-	-	6	III
2	EC 6299	Project phase-II				8	IV
		Total contact hours/Credits	-	-	-	14	---

Elective I

S. N.	Code	Subject	*Prerequisites, if any*
1.	EC 5231	Design and Synthesis using Verilog HDL	---
2.	EC 5232	Nanoelectronics	---
3.	EC 5233	Embedded System	---
4.	EC 5234	VLSI DSP Design	---
5.	EC 5235	Semiconductor Optoelectronics, theory & Design	---

Elective II

S. N.	Code	Subject	*Prerequisites, if any*
1.	EC 5241	ASIC design & FPGA	---
2.	EC 5242	Foundations of VLSI CAD	---
3.	EC 5243	MEMS Analysis	---
4.	EC 5244	Low Power VLSI	---
5.	EC 5245	RF Design	---

Elective III

S. N.	Code	Subjects	*Prerequisites, if any*
1.	EC 5251	AC Analysis of MOS	EC 5203
2.	EC 5252	Advanced VLSI Interconnects	--
3.	EC 5253	Mixed mode VLSI Circuits	EC 5202
4.	EC 5254	High Frequency Semiconductor Devices and Circuits	EC 5201
5.	EC 5255	System on Chip	EC 5202

Elective IV

S. N.	Code	Subject	*Prerequisites, if any*
1.	EC 5261	Solar Photovoltaics and Thin Film Technology	EC 5201
2.	EC 5262	Reconfigurable Hardware Design	EC 5202
3.	EC 5263	Advanced CMOS Devices and Technology	EC 5201
4.	EC 5264	Flexible Electronics	EC 5201
5.	EC 5265	Optimization Techniques in Engineering	---

Detailed Syllabi

EC-5201	SEMICONDUCTOR DEVICE PHYSICS	L	T	P	C
	M.Tech. (MVD), First Semester (Core)	3	0	0	3

Introduction to semiconductor physics: review of crystal structure and harmonic wave motion, evolution of quantum mechanics, Schrodinger's wave theory, bound and scattering states, quantum tunneling, one electron theory – Bloch theorem, Kronig-Penney model, crystal momentum and effective mass, 3D lattice – $E-k$ diagram, allowed and forbidden bands, density of states, carrier statistics and distribution functions, generation and recombination - excess carriers in semiconductors, Boltzmann transport equation, Continuity equation, Poisson's equation and their solution; High field effects: velocity saturation, hot carriers and avalanche breakdown.

Semiconductor junctions: Schottky and Ohmic contacts, homo- and hetero-junction band diagrams and I-V characteristics, small signal switching models.

Texts/References:

1. D. J. Griffiths , Introduction to Quantum Mechanics
2. D. A. Neamen, Semiconductor Physics and Devices
3. R. L. Liboff, Introductory Quantum mechanics
4. N. W. Ashcroft and N. D. Mermin, Solid State Physics
5. J. P. Mckelvey, Solid State and Semiconductor Physics, Harper and Row, 1966.
6. D.K. Schroder, Semiconductor Material and Device Characterization, John Wiley, 1990.
7. C.T. Sah, Fundamentals of Solid-State Electronic Devices, Allied Publishers and World Scientific, 1991.
8. E.F.Y. Waug, Introduction to Solid-State Electronics, North Holland, 1980

COs:

The students will be able to:

1. Apply the fundamental principles and applications of modern electronic and semiconductor devices
2. Analyze the basic semiconductor device physics and its application to other devices
3. Demonstrate quantum mechanics and its applications in semiconductor devices.
4. Illustrate band engineering

EC-5202	DIGITAL VLSI DESIGN	L	T	P	C
	M.Tech. (MVD), First Semester (Core)	3	0	0	3

Review of MOSFET operation and CMOS process flow: MOS Threshold voltage, MOSFET I-V characteristics: Long and short channel, MOSFET capacitances, lumped and distributed RC model for interconnects, transmission lines, CMOS process flow, Layout and design rules.

CMOS inverter: Static characteristics, power consumption, dynamic behavior, buffer design using the method of logical effort.

Combinational logic: Transistor sizing in static CMOS logic gates, static CMOS logic gate sizing considering method of logical effort, dynamic logic, pass-transistor logic, common mode and other cross-coupled logic families.

Sequential logic: Static latches and flip-flops (FFs), dynamic latches and FFs, sense-amplifier based FFs, NORA-CMOS, Schmitt trigger, monostable and astable circuits.

Memories and array structures: MOS-ROM, SRAM cell, memory peripheral circuits

Texts/References:

1. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, "Digital Integrated Circuits: A Design Perspective," Prentice Hall, 2003.
2. Sung-Mo Kang, Yusuf Liblebici, "CMOS Digital Integrated Circuits," Tata Mc Graw Hill, 2003.
3. R. Jacob Baker, "CMOS Mixed-Signal Circuit Design," Wiley India Pvt. Ltd, 2009
4. Ivan Sutherland, R. Sproull and D. Harris, "Logical Effort: Designing Fast CMOS Circuits", Morgan Kaufmann, 1999.

COs:

On successful completion of the course a student will be able to:

1. Design a CMOS inverter meeting the static and dynamic performance characteristics.
2. Design combinational logic circuits (both static and dynamic) in CMOS.
3. Design sequential logic circuits in CMOS.
4. Design various Arithmetic Building Blocks.
5. Understand the timing issues in Digital Circuit Design and apply them.
6. Carryout the layout design using CAD tools.

EC-5203	DEVICE MODELLING	L T P C
	M.Tech. (MVD), First Semester (Core)	3 0 0 3

Contact Potentials: Overview.

Two-terminal MOS structure: flat-band voltage, potential and charge balance, channel charge, accumulation, depletion, inversion, threshold voltage, small signal capacitances.

Three-terminal MOS structure: effect of channel-body potential, body effect, inversion regions, contacting the inversion layer, region of inversion: approximate limits, threshold voltage, V_{CB} control point of view, pinch-off voltage.

Four-terminal MOS Transistor: Complete charge-sheet model, simplified charge-sheet model, strong and weak inversion approximation to the channel current, effective surface mobility, field dependence of the surface mobility, breakdown.

Small-Dimensional Effects: Long- and short-channel MOS transistor, carrier velocity saturation, channel length modulation, charge sharing, DIBL, threshold voltage rolls-off, narrow channel effects, punch

through, hot-carrier effects, GIDL, scaling: constant field and constant voltage scaling, non-scaling effects, modern scaling.

Texts/References:

1. Yannis Tsividis, Operation and Modeling of the MOS Transistor, Oxford University Press.
2. N. Arora, MOSFET models for VLSI Circuit Simulation, Springer-Verlag.
3. Ning and Taur, Fundamentals of modern VLSI devices, Oxford University press.

COs:
The students will be able to:

1. Analyse MOS and its operation on the basis of physical operation
2. Develop a physics based knowledge on the basic fundamentals in the course
3. Relate a 2nd order effect or deviation from ideal behaviour in circuit level to device physics concept learnt in the course
4. Understand, articulate and demonstrate new ideas given in research literature of the field

EC-5204	VLSI Lab – I	L T P C
	M.Tech. (MVD), First Semester lab	0 0 3 2

The laboratory course consists of experiments related to Digital IC design using cadence tool and FPGA based design.

1. Verify the voltage transfer characteristics and transient analysis of CMOS Inverter.
2. Design & simulation of serial binary adder.
3. Design & simulation of SRAM.
4. Design & simulation of barrel shifter
5. Design & simulation of multiplier

Note: The above experiments (1-5) require layout design and simulation also.

6. Implement half Adder/full adder using FPGA.
7. Implement D/T Flip flop using FPGA
8. Implement ALU using FPGA
9. Implementation of vending machine using FPGA
10. Implementation of MIPS processor using FPGA

COs:

The graduates will be able to:

1. Understand the design mechanisms of various digital circuits and systems.
2. Analyze the characteristics of operations such as adders, multipliers, and shifters.
3. Observe various operations practically in FPGA
4. Design FPGA based systems for various specifications and applications.
5. Design innovative circuits/systems at IC level and system level

EC5210	Seminar	L T P C
	M.Tech. (MVD), First Semester	0 0 2 1

COs:

The students will be able to:

1. Analyze current trends in Microelectronics and VLSI technologies
2. Evaluate the potential applications in local contexts.
3. Improve presentation skills
4. Demonstrate the effective use of present research findings clearly and persuasively.
5. Apply critical thinking skills to propose innovative solutions to a real-world case study discussed during the seminar.

Elective – I

EC-5231	Design and Synthesis using Verliog HDL	L T P C
	M.Tech. (MVD), First Semester (Elective – I)	3 0 0 3

Design Concepts – Digital Hardware, Design Process, and Design of digital hardware, Introduction to CAD tools, and introduction to verilog/VHDL.

Logic system, data types and operators for modeling in verilog HDL. Verilog Models of propagation delay and net delay path delays and simulation, inertial delay effects and pulse rejection. Behavioral descriptions in Verilog HDL.

Synthesis of combinational logic – multiplexers, decoders, encoders, code converters, arithmetic comparison circuits, verilog/vhdl for combinational circuits.

Synthesis of Sequential logic- Flip-Flops- SR, D, Master slave edge triggered D, T, JK, registers – shift registers, parallel access shift registers, counters – asynchronous, synchronous, counters with parallel load, reset synchronization, other counters, simple processor

Synchronous sequential circuits – basic design steps, state assignment problem, serial adder, state minimization, design of counter using the sequential circuit approach, FSM as an arbiter circuit, ASM.

Asynchronous Sequential Circuit – Analysis and synthesis of asynchronous circuits, state assignment, state reduction, hazards

Testing of Logic circuits – Fault models, path sensitizing, built-in self-test (BIST),

Text Books

1. M.D.Ciletti, “Modeling, Synthesis and Rapid Prototyping with the Verilog HDL”, PHI, 1999.
2. S. Palnitkar, “Verilog HDL – A Guide to Digital Design and Synthesis”, Pearson, 2003.

Reference Books

1. J Bhaskar, “A Verilog HDL Primer (3rd edition)”, Kluwer, 2005.
2. M.G.Arnold, “Verilog Digital – Computer Design”, Prentice Hall (PTR), 1999.
3. Recent literature in Modeling and Synthesis with Verilog HDL.

COs:

The students will be able to:

1. Understand the basic concepts of verilog HDL
2. Model digital systems in verilog HDL at different levels of abstraction
3. Know the simulation techniques and test bench creation.
4. Understand the design flow from simulation to synthesizable version
5. Get an idea of the process of synthesis and post-synthesis

EC-5232	Nanoelectronics	L T P C
	M.Tech. (MVD), First Semester (Elective – I)	3 0 0 3

Classification of Materials and Devices, Various Semiconductor materials and their advantages & disadvantages, Properties of Semiconductor, Band model for semiconductors, bonding forces and energy bands in solids, charge carriers in semiconductors. MOS Scaling theory, Issues in scaling MOS transistors: Short channel effects, Requirements for Non classical MOS transistor. Solid State Devices.
Schottky and Ohmic contact, Tools used for Nanoelectronics, Fabrication/ Synthesis techniques of thin film devices, Characterization of thin film devices.

Texts/References:

1. S.M. Sze, “Physics of semiconductor devices”, Wiley Pub.
2. B.G. Streetman, “Solid State Electronics Devices”, Prentice Hall, 2002.
3. M.S.Tyagi, “Semiconductor Materials and Devices,” Wiley Pub.
4. D. J. Griffiths , Introduction to Quantum Mechanics
5. D.K. Schroder, Semiconductor Material and Device Characterization, John Wiley, 1990.
6. C.T. Sah, Fundamentals of Solid-State Electronic Devices, Allied Publishers and World Scientific, 1991.

COs:

The students will be able to:

1. Analyze the energy band models of semiconductor devices
2. Apply the concept of non-classical MOS transistor to solve the issues associated with scaling
3. Implement Schottky and Ohmic contact to realize advanced FET devices
4. Determine suitable fabrication process to grow thin film devices
5. Demonstrate tools to characterize thin film devices

EC-5233	Embedded system	L T P C
	M.Tech. (MVD), First Semester (Elective – I)	3 0 0 3

Introduction: Embedded system Overview, Design challenge, processor Technology, IC Technology, Full custom, VLSI Design technology (Compilation/Synthesis), Custom Single–purpose Processor: Hardware Transistor and logic gate custom single purpose processor design, Optimizing custom single-purpose processor design, Bus architecture

General purpose Processor: Basic architecture, Operation, Programmer view, Development environment, ASIP micro controller, Bus architecture.

Standard single purpose processor: Timer, counter, UART, LCD Controller, Key pad controller, Stepper motor controller.

Memory Technology, Multilevel Bus Architecture, Interface technology, Parallel /Serial Communication Technology, Serial protocols (I^2C, CAN, USB, Parallel protocols PCI BUS, ARM Bus.

References:

1. Embedded System Design by Vahid/Givargis
2. The Power PC Architecture - Cathy May and Ed Silha, Morgan Kauffmann, 1998.
3. The Programming Environment for 32-Bit Microprocessors - Motorola
4. MPC860 User's Manual - Motorola.
5. An Implementation guide to Real Time Programming - David L. Ripps, Yourdon Press, 1990.
6. Programming Microsoft Windows CE - Douglas Boling, Microsoft Press, 2001.
7. Building Powerful platform with Windows CE - James Y. Wilson and Havewala, Addison Wesley, 2001.
8. Embedded Systems : Architecture, Programming and Design- RajKamal, TMH,2003
9. Frank Vahid and Tony Givargis, Embedded system design: A unified hardware/software introduction, John Wiley and Sons, 2002.

COs:

The students will be able to:

1. Understand the various specifications and applications of embedded systems
2. Analyze the general purpose processor architecture and its development.
3. Implement an embedded application using interfacing blocks such as digital camera, alarm clock etc.
4. Ability to design an embedded real time system using Multilevel Bus Architecture.

EC-5234	VLSI DSP Design	L T P C
	M.Tech. (MVD), First Semester (Elective – I)	3 0 0 3

Computational characteristics of DSP algorithms and applications; their influence on defining a generic instruction-set Architecture for DSPs.

Architectural requirement of DSPs: high throughput, low cost, low power, small code size, embedded applications. Techniques for enhancing computational throughput: parallelism and pipelining.

Data-path of DSPs: multiple on-chip memories and buses, dedicated address generator units, specialized processing units (hardware multiplier, ALU, shifter) and on-chip peripherals for communication and control.

Control-unit of DSPs: pipelined instruction execution, specialized hardware for zero-overhead looping, interrupts.

Architecture of Texas Instruments fixed-point and floating-point DSPs: brief description of TMS320 C5x /C54x/C3x DSPs; Programmer's model.

Architecture of Analog Devices fixed-point and floating-point DSPs: brief description of ADSP 218x / 2106x DSPs; Programmer's model.

Advanced DSPs: TI's TMS 320C6x, ADI's Tiger-SHARC, Lucent Technologies' DSP 16000 VLIW processors. Applications: a few case studies of application of DSPs in communication and multimedia.

References:

1. P. Pirsch: Architectures for Digital Signal Processing; John Wiley, 1999.
2. R. J. Higgins: Digital Signal Processing in VLSI; Prentice-Hall, 1990.
3. Texas Instruments TMSC5x, C54x and C6x Users Manuals.
4. Analog Devices ADSP 2100-family and 2106x-family Users Manuals.
5. K. Parhi: VLSI Digital Signal Processing Systems; John Wiley, 1999.
6. K. Parhi and T. Nishitani: Digital Signal Processing for Multimedia Systems; Marcel Dekker, 1999.
7. IEEE Signal Processing Magazine: Oct 88, Jan 89, July 97, Jan 98, March 98 and March 2000.

COs:

The students will be able to

1. Illustrate the fundamental concept of computational Characteristics of DSP algorithms
2. Analyze the architectures of DSPs.
3. Demonstrate the data path of DSPs
4. Illustrate the pipelining instructions
5. Demonstrate the fixed point and floating point DSPs.
6. Analyze the advanced processors.

EC-5235	**Semiconductor Optoelectronics, theory & Design**	**L T P C**
	M.Tech. (MVD), First Semester (Elective – I)	3 0 0 3

Introduction:

Energy levels & bands in solids, Spontaneous & stimulated transitions, the creation of light Transverse confinement of carriers and photons in Diode Lasers, the double Hetero structure Semiconductor materials

for Diode Lasers, Epitaxial Growth Technology, Lateral confinement of current carriers and photons for practical lasers.

A Phenomenological approach to Diode Lasers:

Carrier generation and recombination in active regions, Spontaneous photon generation and LED, Photon generation and loss in laser cavities, Threshold or steady state gain in lasers, Threshold current and Power out vs. current, Relaxation resonance and frequency response, Characterizing real Diode Lasers.

Mirrors and Resonator for Diode Lasers:

Scattering theory, S and T matrices for some common elements, three and four mirror laser cavities.

Gratings, DaR Lasers and DFB Lasers: Mode suppression ratio in single frequency lasers.

Gain and Current relations: Introduction, Radiative transitions, Optical gains, Spontaneous -emission. Non-radiative transitions, Active materials and their characteristics.

Dynamic Effect: The rate equation, Steady state solutions, Steady state multimode solutions, Differential analysis of the rate equations, large signal analysis. Relative intensity noise and line width, Carrier transport effect, feedback effect.

Perturbation and Coupled Mode Theory:

Dielectric Waveguide:

Introduction, plane wave incident on a planar dielectric boundary, dielectric waveguide analysis technique, guided mode power and effective width, Radiation losses for nominally guided mode.

Topics in the Application of Diode Lasers in Fiber Optic Communication.

Texts/References:

1. Larry A Coldren & S W Corzine: Diode Lasers & Photonic Integrated Circuits, Willey Interscience ISBN : 04711 18753
2. S L Chuang: Physics of Optoelectronic Devices, Willey Interscience ISBN: 0471109398.
3.

COs:

1. An understanding of semiconductor material properties and semiconductor optoelectronic device physics.
2. Gain in-depth knowledge on the diode laser properties, operation, and fabrication.
3. Understand various structures of laser diode through scattering matrix formalism.
4. Gain knowledge on differential analysis of the rate equations.
5. Learn about dielectric waveguide: a key components of modern integrated optics.

Elective -II

EC-5241	ASIC design & FPGA	L T P C
	M.Tech. (MVD), First Semester (Elective – II)	3 0 0 3

Introduction to ASICs and FPGAs, Fundamentals in digital IC design, FPGA & CPLD Architectures, FPGA Programming Technologies, FPGA Logic Cell Structures, FPGA Programmable Interconnect and I/O Ports, FPGA Implementation of Combinational Circuits, FPGA Sequential Circuits, Timing Issues in FPGA Synchronous Circuits, Introduction to Verilog HDL, FPGA design flow with Verilog HDL, FPGA Arithmetic Circuits, FPGAs in DSP Applications, FPGA Microprocessor design, Design Case Studies, FPGA High-level Design Techniques, Programming FPGAs in Electronic Systems, Dynamically Reconfigurable Systems, Latest Trends in Programmable ASIC and System Design.

References:

1. Wayne Wolf, FPGA -Based System Design, Prentice Hall, 2004
2. M. D. Ciletti, Advanced Digital Design with Verilog HDL, Prentice Hall, 2002
3. John P. Hayes, Computer Architecture and Organization, Third Edition, McGraw-Hill, 1998
4. Michael Smith, Application-Specific Integrated Circuits, Addison-Wesley, 1997
5. Keshab K. Parhi, VLSI Digital Signal Processing Systems: Design and Implementation, Wiley, 1998
6. Xilinx User Manuals and Application Notes

COs:

The students will be able to:

1. Learn VHDL & Verilog coding, latest trends in programming ASIC.
2. Apply VHDL & Verilog coding for implementation of combinational and sequential circuits.
3. Design and implement logic systems simulation, especially the design and use of test benches.
4. Implement various real time case studies in FPGA and ASIC.

EC-5242	Foundations of VLSI CAD	L T P C
	M.Tech. (MVD), First Semester (Elective – II)	3 0 0 3

Layout Environment, layout methodologies, packaging, Delay models, rise-time & fall time delay, Gate delay, Power Dissipation, Static & Dynamic power dissipation, total power dissipation, power minimization.

Design Strategies, Design Synthesis.
Placement - portioning, floor-planning, placement.
Routing – Global & Detailed Routing, Routing in FPGA.
Design Verification & Testing.

References:

1. M. Sarrafzadeh & C.K Wong – An Introduction to Physical VLSI Design
2. Neil Weste & K Eshraghian – Principles of CMOS VLSI Design.

COs:

On successful completion of the course a student:

1. Will be able to partition a given logic circuits using CAD tools to meet the cost function and other constraints.
2. Will be able to solve the floor planning and placement issues in circuit layout using appropriate CAD tools.
3. Will be able to analyze the physical design requirements and find the most appropriate routing path for the modules inside the chip.
4. Will be able to carry out all the physical verification (such as DRC rules, LVS, ERC etc.) of the layout designed.

EC-5243	**MEMS Analysis**	**L T P C**
	M.Tech. (MVD), First Semester (Elective – II)	3 0 0 3

Introduction: What is MEMS? Unique Characteristics of MEMS and Typical Application Areas of MEMS

IC fabrication vs. MEMS Fabrication: Deposition, lithography, oxidation, etching, Plasma etching, Sputtering, RIE, 1, 2 and 3 mask level processes, wet etching (anisotropic and isotropic), crystal directions in Si, Bulk micro-machining, Surface micro-machining, wafer bonding, Electroplating, Molding etc.

Introduction to Beam Mechanics: Relationship between tensile stress and stain- mechanical properties of silicon and thin films, Flexural beam bending analysis under single loading condition- Types of beam-deflection of beam-longitudinal stain under pure bending spring constant, torsional deflection, intrinsic stress, resonance and quality factor.

Sensing and Actuation: Electrostatic sensing and actuation-parallel plate capacitor – Application-Inertial, pressure and tactile sensor parallel plate actuator- comb drive.

Thermal sensing and Actuations-thermal sensors-Actuators- Applications- Inertial, Flow and Infrared sensors.

Piezoresistive sensors- piezoresistive sensor material- stress in flexural cantilever and membrane Application-Inertial, pressure, flow and tactile sensor.

Piezoelectric sensing and actuation- piezoelectric material properties-quartz-PZT-PVDF –ZnO Application-Inertial, Acoustic, tactile, flow-surface elastic waves

Magnetic actuation- Micro magnetic actuation principle- deposition of magnetic materials-Design and fabrication of magnetic coil.

Electrothermal MEMS: Flow Sensors, Gas Detectors, Uncooled Infrared Sensors, Bimorph Actuators, Bent-Beam Actuators.

RF MEMS: Switches, active and passive components, static and dynamic modeling.

CMOS-MEMS Integration: Overview, different techniques, packaging and integration.

Overview of BioMEMS, Microfluidics: Biosensor and BioMEMS; Microfluidics; Digital Microfluidics; Ink jet printer.

Text/References

1. Chang Liu, Foundations of MEMS, Pearson Education Asia, 2012.
2. S. D. Senturia, Microsystem Design, Springer, India, 2006.

COs:
The students will be able to:

1. Familiar with the fundamentals, fabrication process and applications of MEMS.
2. Understand the basic principles of MEMS sensors and actuators (mechanical, electrical, piezoresistive, piezoelectric, thermal, microfluidic).
3. Apply knowledge of beam mechanics and material properties for the design of various sensors and actuators.
4. Prepare the knowledge base of various MEMS sensors and actuators.
5. Implement various applications of MEMS in Bio medical field and healthcare domain.
6. Investigate CMOS-MEMS integration in VLSI domain.

EC-5244	Low Power VLSI	L T P C
	M.Tech. (MVD), First Semester (Elective – II)	3 0 0 3

Introduction: Introduction, Motivation for low power design, need and application low power design, Low power design space: voltage, Physical Capacitance, Switching Activity.

Sources of power consumption and Power estimation: Static power and dynamic power: switching component of power, short circuit component of power, leakage component of power and other component of power consumption. Power estimation considering node transition activity factor, glitching effect and glitching power

Voltage Scaling approaches for low power design: reliability driven voltage scaling, technology driven voltage scaling, energy-delay minimum based voltage scaling, voltage scaling through threshold reduction, architecture driven voltage scaling.
Adiabatic Switching for low power design: concept of adiabatic charging, adiabatic amplification. Adiabatic logic gates, stepwise charging, pulsed power supply.

Switching Capacitance minimization for low power design: Algorithmic approaches, Architecture optimization, Logic optimization, Circuit optimization, physical design optimization.

Low power adder design: introduction, Standard adder: half adder, full adder, CMOS adder architectures: Ripple carry adder (RCA), Carry look- Ahead adder (CLA), Carry Select Adder (CSL), Carry Save Adder (CSA), Carry Skip Adder (CSK), Conditional Sum Adder (COS), Performances of all the adders with low power design, BiCMOS adders.

Texts/References

1. Low Power Digital CMOS Design - Anantha P. Chandrakasan and Robert W. Broderson.
2. Low Power CMOS VLSI Circuit Design- Kaushik Roy and Sarat C. Prasad
3. Low – Voltage, Low – Power VLSI Subsystems"- Kiat-Seng Yeo and Kaushik Roy.

COs:

The students will be able to:

1. Compare various sources of power dissipation.
2. Understand voltage scaling approaches for low power design.
3. Apply adiabatic switching for low power design.
4. Analyze switching activities involved in MOSFET's and different power dissipation mechanisms involved thereby.
5. Design various low power designs such as Conditional Sum Adder, Carry Save adder etc.

EC-5245	RF Design	L T P C
	M.Tech. (MVD), First Semester (Elective – II)	3 0 0 3

Passive/active IC devices, Passive RLC network, Distributed systems, Smith chart, Bandwidth estimation tech., RF amplifier design, Voltage reference & biasing, Noise, LNA design, Mixers, RF power amplifiers, Feedback systems, Phase-locked loop, Oscillator, synthesizer, Phase noise, Resonant Circuits, Filter Design, Impedance Matching, The Transistor at Radio Frequencies, Small-Signal RF Amplifier Design, RF Power Amplifiers.

Texts/References:

1. R. Ludwig and P. Bretchko, RF Circuit Design. Prentice Hall, 2000.
2. Chris Bowick, RF Circuit Design, Newens, 1997.

COs:

The students will be able to:

1. Recognize the limitations of existing passive and active circuits at microwave frequencies.
2. Study the performance of RF circuits using Analytical/Graphical Approach.
3. Understand the designing of passive circuits (impedance matching circuits, filter circuits, etc.).
4. Understand the designing of active circuits (amplifier circuits, oscillator circuits, etc.).

SECOND SEMESTER

EC-5211	Analog VLSI Design	L	T	P	C
	M.Tech. (MVD), Second Semester (Core)	3	0	0	3

Introduction to CMOS analog circuits, MOS transistor DC & AC small signal parameters from large signal model, common source amplifier with various loads, source follower, common gate amplifier, cascade amplifier, folded cascade, frequency response, stability, and noise issues of amplifiers, current/ source/ sink mirror. Matching, Wilson current source and regulated current source, Band-gap reference, Differential amplifier, Op-Amp, Design of Op-Amp. Sense amplifier, Sample and Hold, Sampled Data Circuits, Switched capacitor filters, DAC, ADC.

Texts/References:

1. B Razavi-Design of Analog Integrated Circuits, Tata McGraw Hill.
2. B. Razavi- RF Microelectronics, Prentice Hall.
3. R.Jacob Baker, H.W.Li, and D.E Boyce CMOS Circuit Design, Layout and Simulation, Prentice-Hall of India, 1998
4. Mohammed Ismail and Terri Faiz- Analog VLSI Signal and Information Process, McGraw-Hill Book Company, 1994
5. Paul R. Gray and R.G Meyer, Analysis and design of Analog Integrated Circuits, John-Wily and sons, USA, (3^{rd} edtn.),1993
6. Journals: IEEE Journal of Solid State Circuits.

COs:

1. Analyze and design a single stage and multi-stage MOS amplifier.
2. Carryout frequency domain analysis and stability analysis of MOS amplifier.
3. Design 2-stage and folded cascade Op-Amp to meet the given specifications.
4. Understand the theory and working principle of sample and hold circuit.
5. Design switched capacitor filter circuits.

EC-5212	VLSI System Testing & Verifications	L	T	P	C
	M.Tech. (MVD), Second Semester (Core)	3	0	0	3

Fundamentals of VLSI Testing

Basic of VLSI testing, Scope of testing and verification in VLSI design process, Issues in test and verification of complex chips, embedded cores and SOCs.

Fault Modeling and Testing

Fault models, fault detection and redundancy, fault equivalence and fault location, fault dominance, automatic test pattern generation, Design for testability, Scan design, Test interface and boundary scan. System testing and test for SOCs. Delay fault testing.

Test Automation and Design Verification

BIST for testing of logic and memories, Test automation, Design verification techniques based on simulation, analytical and formal approaches.

Functional and Timing Verification

Functional verification, Timing verification, Formal verification, Basics of equivalence checking and model checking, Hardware emulation.

Texts/References:

1. M. L. Bushnell and V.D. Agrawal, Essentials of Electronic Testing for Digital Memory and Mixed Signal VLSI Circuits, Springer, 2005
2. T. Kropf, Introduction to Formal Hardware Verification, Springer Verlag, 2000
3. M. Huth and M. Ryan, Logic in Computer Science, Cambridge Univ. Press, 2004
4. M. Abramovici, M. Breuer, and A. Friedman, Digital System Testing and Testable Design, IEEE Press, 1994.

COs:

The students will be able to:

1. Apply the concepts in testing which can help them design a better yield in IC design.
2. Tackle the problems associated with testing of semiconductor circuits at earlier design levels so as to significantly reduce the testing costs.
3. Analyse the various test generation methods for static & dynamic CMOS circuits.
4. Identify the design for testability methods for combinational & sequential CMOS circuits.
5. Recognize the BIST techniques for improving testability.

EC-5213	VLSI Technology	L	T	P	C
	M.Tech. (MVD), Second Semester (Core)	3	0	0	3

Environment for VLSI Technology: Clean room and safety requirements, Water cleaning processes & wet chemical etching techniques.

Impurity incorporation: solid state diffusion modeling & technology: Ion implantation modeling, technology & damage annealing, Characterization of impurity profiles.

Oxidation: Kinetics of Silicon dioxide growth both for thick, thin & ultrathin films. Oxidation technologies in VLSI & ULSI: Characterization of oxide films; High K and low k dielectrics for ULSI.

Lithography: Photolithography-beam lithography & newer lithography techniques for VLSI/ULSI; Mask Generation

Chemical Vapor Deposition Techniques: CVD techniques for deposition of polysilicon, silicon dioxide, silicon nitride & metal films; Epitaxial growth of silicon; modeling & technology.

Metal Film Deposition: Evaporation & sputtering techniques. Failure mechanisms in metal interconnects; multilevel metallization schemes.

Plasma & Rapid Thermal Processing: PECVD, Plasma etching & RIE techniques; RTP techniques for annealing, growth & deposition of various films for use in ULSI.

Process Integration for NMOS, CMOS & Bipolar Circuits: Advanced MOS technologies

Text/References:

1. C.Y. Chang &S.M.Sze(Ed), ULSI Technology, McGraw Hill Companies Inc, 1996.
2. S.K.Gandhi, VLSI Fabrication Principles, John Inc., New York, 1983
3. S.M.Sze(Ed), VLSI Technology, 2nd edition, McGraw Hill, 1988.

COs:

The students will be able to:

1. Understand about clean room and its safety measures
2. Learn about cleaning of semiconductor wafers and role of the crystal structures in epitaxial growth
3. Understand and analyse the theory of various state-of-art fabrication techniques associated with semiconductor devices fabrication and related instruments' working principle
4. Apply the knowledge of fabrication process flow of semiconductor devices for emerging VLSI applications
5. Interpret the main challenges in fabrication industry and select suitable growth technique in a given range of constraints.

EC-5214	**VLSI Lab II**	**L T P C**
	M.Tech. (MVD), Second Semester lab	0 0 3 2

The laboratory course experiments are related to simulation of analog circuits using Cadence tool, and device simulation using Sentaurus TCAD.

1. Design of single stage amplifier
2. Design of current mirror
3. Design of differential amplifier
4. Design an Op-amp
5. Design of Comparator

Note: For the above experiments (1-5) complete the design flow as mentioned below:
a. Draw the schematic and verify the following:
i) DC Analysis ii) AC Analysis iii) Transient Analysis
b. Draw the Layout and verify the DRC, ERC.
c. Check for LVS and Extract RC and back annotate the same and verify the design.

6. To design a Bulk MOSFET using Sentaurus TCAD and check its I_{ON}/I_{OFF}, SS and I_D vs. V_{GS} characteristics.
7. To design a Double Gate MOSFET using Sentaurus TCAD and check its I_{ON}/I_{OFF}, SS and I_D vs. V_{GS} characteristics.
8. To design a SOI MOSFET using Sentaurus TCAD and check its I_{ON}/I_{OFF}, SS and I_D vs. V_{GS} characteristics.
9. To design a TFET using Sentaurus TCAD and check its I_{ON}/I_{OFF}, SS and I_D vs. V_{GS} characteristics.
10. To design a HEMT using Sentaurus TCAD and check its I_{ON}/I_{OFF}, SS and I_D vs. V_{GS} characteristics.

COs:
The students will be able to

1. Find the performance analysis of various analog circuits
2. Simulate OP-amp, Comparator and their applications in schematic and layout level.
3. Analyze various devices performance parameters in device simulator
4. Innovate new device and verify the same in various circuits.

EC 5220	Colloquium	L T P C
	M.Tech. (MVD), Second Semester	0 0 2 1

COs:

The student will be able to:

1. Understand the research findings using clear, concise, and audience-appropriate language.
2. Depict the presentations by identifying strengths, weaknesses, and areas for improvement.
3. Enhance in scholarly discussion by asking insightful questions and providing constructive feedback.
4. Integrate interdisciplinary perspectives into their own research or professional practice.

Elective-III

EC-5251	AC Analysis of MOS	L T P C
	M.Tech. (MVD), Second Semester (Elective – III)	3 0 0 3

Large Signal modeling:
Quasi-static operation, terminal currents in quasi-static operation, charge partitioning, charging currents, evaluation of intrinsic charges, transit time, limitations of quasi-static models, extrinsic capacitances and resistances, drain-source charge partitioning.

Small Signal low and medium frequency modeling:
Intrinsic modeling: drain-to-source current, gate and body currents, complete low-frequency small signal model, various conductances in various regions of operations, effect of extrinsic resistances. Medium frequency small signal modeling for the intrinsic part, intrinsic transition frequency, small dimensional effects, noise analysis.

High frequency small signal modeling:
Quasi-static modeling: intrinsic capacitances, small signal equivalent circuit, capacitance evaluations. Non-quasi-static modeling and high frequency noise, RF modeling.

Circuit simulation modeling:
Various types of models, device modeling for circuit simulation, general considerations and choices, parameter extraction, introduction to common circuit simulation models.

Texts/References

1. Operation and modeling of the MOS transistor — Tsividis and McAndrew
2. MOSFET Models for VLSI Circuit Simulation — N. Arora
3. Fundamentals of Modern VLSI Devices — Taur and Ning

COs:
The students will be able to:

1 Articulate the need for quasi-static operations of MOS
2 Interpret the fundamental behavior of MOS when excited by ac signal superimposed with DC bias supplies
3 Demonstrate frequency limitations vis-à-vis derivation of AC parameters of MOS
4 Identify various conductive and capacitive effects in various (low, medium, and high) frequency ranges
5 Express proficiency in general considerations and choices for common circuit simulation tools

EC-5252	Advanced VLSI interconnects	L T P C
	M.Tech. (MVD), Second Semester (Elective – III)	3 0 0 3

Preliminary concepts: Interconnects for VLSI applications, metallic interconnects, optical interconnects, superconducting interconnects, advantages of copper interconnects, challenges posed by copper interconnects, fabrication process, even and odd mode capacitances, miller theorem, transmission line equations, resistive interconnection as ladder network, propagation modes in microstrip interconnection, slow wave mode propagation, propagation delays.

Parasitic extraction: Parasitic resistance, effect of surface/interface scattering and diffusion barrier on resistance, Capacitance: parallel-plate capacitance, fringing capacitance, coupling capacitance, methods of capacitance extraction, Inductance: self inductance, mutual inductance, methods of inductance extraction, high frequency losses, frequency dependent parasitics, skin effect, dispersion effect.

Modeling of interconnects and Crosstalk analysis: Elmore model, Transfer function model, even and odd mode model, Time domain analysis of multi conductor lines, Finite Difference Time Domain (FDTD) method, performance analysis using linear driver (Resistive) and nonlinear driver (CMOS), advanced interconnect techniques to avoid crosstalk.

Carbon nanotube and Graphene nanoribbon VLSI interconnects: Quantum electrical properties: quantum conductance, quantum capacitance, kinetic inductance, Carbon nanotube (CNT) and Graphene nanoribbon (GNR) interconnects, electron scattering and lattice vibrations, electron mean free path, single-wall CNT and single layer GNR resistance model, multi-wall CNT and multi-layer GNR resistance model, transmission line interconnect models, performance comparison of CNTs, GNRs and copper interconnects.

Advanced VLSI Interconnects: Optical interconnects, Stretchable interconnects, Superconducting interconnects, Nanotechnology interconnects, Silicon nanowires: system issues and challenges, material processing issues and challenges, design issues and challenges.

Texts/References:

1. Ashok K. Goel, High-Speed VLSI Interconnects, 2007.
2. Y.S. Diamand, Advanced Nanoscale ULSI Interconnects: Fundamentals and Applications, 2009.
3. H.S Philip Wong and Deji Akinwande, Carbon nanotube and Graphene Device Physics, 2011.

COs:

The students will be able to:

1. Understand device and interconnect scaling related issues.
2. Extract various parasitic components of interconnects for signal integrity analysis
3. Perform RC/RLC based Interconnect analysis in terms of delay, crosstalk etc.
4. Solve various problems/challenges in advanced VLSI interconnects

EC-5253	Mixed Mode VLSI Circuits	L T P C
	M.Tech. (MVD), Second Semester (Elective – III)	3 0 0 3

Data converter fundamentals: Analog versus Discrete Time Signals, Sample and Hold Characteristics, DAC Specifications, ADC Specifications, Mixed-Signal Layout Issues

Data Converters Architectures: DAC Architectures, Digital Input Code, Resistors String, R-2R Ladder Networks, Current Steering, Charge Scaling DACs, Cyclic DAC, Pipeline DAC, ADC Architectures, Flash, 2-Step Flash ADC, Pipeline ADC, Integrating ADC, Successive Approximation ADC

Non-Linear Analog Circuits: Basic CMOS Comparator Design, Analog Multipliers, Multiplying Quad, Level Shifting

Data Converter SNR: Improving SNR Using Averaging, Decimating Filters for ADCs, Interpolating Filters for DAC.

Sub-Microns CMOS circuit design: Process Flow, Capacitors and Resistors, MOSFET Switch, Delay and adder Elements, Analog Circuits MOSFET Biasing, OP-Amp Design

Texts/References:

1. Design, Layout, Stimulation, R. Jacob Baker, Harry W Li, David E Boyce, CMOS Circuit, PHI Edition, 2005
2. CMOS- Mixed Signal Circuit Design, R. Jacob Baker, (Vol. of CMOS: Circuit Design, Layout and Stimulation), IEEE Press and Wiley Inter-science, 2002
3. CMOS Analog Circuit Design**,** P e Allen and D R Holberg, Second Edition, Oxford University Press, 2002

COs:

On successful completion of the course a student:

1. Will be able to design a switched capacitor filter circuit to meet any given specifications.
2. Will understand thoroughly different performance metrics for the sample and hold circuits.
3. Will have a fundamental knowledge of designing comparator using OTA.
4. Will have a thorough knowledge of different specifications of Data Converter.
5. Understand the design methodology of Mixed Signal IC.

6. Will be able to design appropriate DAC and ADC to meet the given specifications.
7. Will have a thorough knowledge of designing PLL.

EC-5254	High-Frequency Semiconductor Devices and Circuits	L T P C
	M.Tech. (MVD), Second Semester (Elective – III)	3 0 0 3

Review of Semiconductor properties - Crystal structure of semiconductors, band theory, occupation statistics, electrical properties, optical properties, recombination kinetics, avalanche process in semiconductors, photon statistics; MESFETs; Transport in low dimensional structures: HEMTs: Hetero-junction BJTs; Design of high frequency amplifiers and oscillators, Resonant tunneling structures, RTD oscillators; Inter-valley scattering, Gunn diodes, IMPATT diodes; TEAPATTs; BARPATTs; mixer diodes; Step recovery diodes; Introduction to epitaxial growth for these structures; elements of device fabrication. LEDs, LASER, detectors, optical amplifiers.

Texts/References

1. Sheila Prasad, Hermann Schumacher, Anand Gopinath, High-Speed Electronics and Optoelectronics: Devices and Circuits, Cambridge University Press, 2009
2. Peter Ashburn, SiGe Hetero-junction Bipolar Transistors, Wiley, 2003
3. WladyslawGrabinski, Bart Nauwelaers, Dominique Schreurs, Transistor Level Modeling for Analog/RF IC Design, Springer, 2006.

COs:
The students will be able to:

1. Apply the fundamentals of crystal structure, energy band theory
2. Illustrate the electrical, optical properties of various devices
3. Analyze devices like MESFET, HEMT, Hetero junction BJT, RTD, Gunn Diodes, IMPATT Diodes, photo detectors
4. Understand the fabrication process flow of various devices
5. Design various circuits such as optical amplifiers, oscillators.

EC-5255	System on Chip	L T P C
	M.Tech. (MVD), Second Semester (Elective – IV)	3 0 0 3

Design of System on a Chip: Introduction, Moore's Law and the consequences, The International roadmap for semiconductor technology, the technology shockwave, and the tide of the markets
BJT Modeling with VBIC: Introduction, VBIC equivalent network, VBIC model formulation, parameter extraction, relationship between SGP and VBIC parameters, VBIC dc modeling, electro-thermal examples, high frequency modeling
A MOS Transistor Model for Mixed Analog-digital Circuit Design and Simulation: Introduction, the long-channel model, the static model for short and narrow geometries, the charge and thermal noise models
MODEL APPLICATION AND EXPERIMENTAL RESULTS: The computer simulation model, Hierarchical model structure, Statistical circuit simulation including matching, The pinch-off voltage measurement and parameter extraction method, Parameter extraction sequence

Efficient Statistical Modeling for Circuit Simulation: introduction, classification of statistical models, hierarchy of statistical variations, process and geometry level modeling, existing statistical modeling approaches, SPICE model parameter perturbation, typical case modeling, distributional statistical modeling, specific case statistical modeling, generic case statistical modeling

Retargetable Application-driven Analog-digital Block Design: Introduction, analog-digital interface requirements, design flow and CAD support, retargetable block design, examples from industry practice

Robust Low Voltage Low Power Analog MOS VLSI Design: Introduction, low voltage CMOS square-law composite cells, statistical VLSI design tools and techniques, statistical design of the CMOS square-law CMOS cells

Ultralow-Voltage Memory Circuits: Introduction, design issues for ultralow-voltage RAMs, DRAM circuits, ultralow-voltage SRAM circuits, perspectives, SOI CMOS technology

Low-voltage Low-power High-speed I/O Buffers: Introduction, PAC, PDC, P-overlap, P-leakage, P-ringing, various types of buffers: CMOS, HSTL, (High-Speed Transistor Logic), GTL/NTL (Gunning Transistor Logic / NMOS Transistor Logic), PCML (Pseudo Current Mode Logic), PECL (Pseudo Emitter Coupled Logic), USB (Universal Serial Bus), Matched-Impedance Buffer, Hyper-LVDS' (Low-Voltage Differential-Signals)

Texts/References

1. Design Of System On A Chip: Devices and Components, Jochen Jess (editor), Ricardo A. L. Reis (editor) Ricardo A. L. Reis, Kluwer Academic Pub, 2004
2. Design of System on a Chip By: Ricardo Reis, Jochen Jess (Eds.), Springer-Verlag, 2004
3. ARM System-on-Chip Architecture (2nd Edition) by Stephen B. Furber, Steve B. Furber, Addison Wesley, Aug. 2000, ISBN: 0201675196.
4. Real-Time Concepts for Embedded Systems, by Qing Li, Caroline Yao, CMP Books, July 2003, ISBN: 157820124.
5. Fundamentals of Embedded Software: Where C and Assembly Meet, by Daniel Wesley Lewis, Prentice Hall, Nov. 2001.

COs:

The students will be able to:

1. Understand the importance of an efficient system-on-chip communication infrastructure
2. Gain knowledge about statistical models, SPICE, SRAM
3. Analyse ultra-low voltage memory circuits.
4. Design low voltage, low power High speed I/O buffers.

Elective-IV

EC-5261	Solar Photovoltaics and Thin Film Technology	L	T	P	C
	M.Tech. (MVD), Second Semester (Elective – IV)	3	0	0	3

Solar Irradiance

Basics of light: properties of light, energy of photon, photon flux, spectral irradiance, radiant power density, black body radiation, sun radiation.

Solar Radiation: The Sun, solar radiation in space, solar radiation outside the earth's atmosphere, terrestrial solar radiation, solar radiation at the earth's surface, atmospheric effects, air mass, motion of the sun, solar time, declination angle, elevation angle, azimuth angle, the sun's position, solar radiation on a tilted surface, arbitrary orientation and tilt, calculation of solar insulation, measurement of solar radiation.

Solar Cells: Evolution of solar cells, Basic principles of solar cell operation: electrical characteristics, optical properties, typical solar cell Structures, ideal efficiency.

Crystalline Silicon Solar Cells: Manufacturing and properties of crystalline silicon, High efficiency laboratory cells, Screen-printed cells, Laser-processed cells, hit cell, rear-contacted Cells, thin silicon solar cells – light trapping, voltage enhancements, silicon deposition and Crystal growth.

Thin-Film Solar Cells: Thin-film Silicon process technologies, hydrogenated amorphous silicon (a-Si:H) layers, Hydrogenated microcrystalline silicon (μSi:H) layers, p-i-n and n-i-p structures, Tandem and Multi-junction solar cells.

Emerging Thin-Film Solar Cells: CdTe based thin film solar cells, $CuInSe_2$ (CIS) based thin-film solar cells, CZTS Solar Cells-crystal structures, thin-film GaAs solar cells, Chalcopyrite based Solar Cells, Concentrator silicon solar cells, Dye-sensitized thin-film solar cells, Perovskite Solar Cell, Organic solar cells, Nanowire Solar Cells.

References

1. Adrian Kitai, Principles of Solar Cells, LEDs and Diodes: The role of the PN junction, John Wiley & Sons, 2011.
2. Augustin McEvoy, L. Castaner, Tom Markvart, Solar Cells: Materials, Manufacture and Operation, 2nd edition, Newnes, 2012.
3. Arvind Shah, Thin-Film Silicon Solar Cells, Illustrated edition, EPFL Press, 2010.
4. I. M. Dharmadasa, Advances in Thin-Film Solar Cells, Illustrated edition, CRC Press, 2012.
5. P. Jayarama Reddy, Solar Power Generation: Technology, New Concepts & Policy, Illustrated edition, CRC Press, 2012.
6. A. Martí, A. Luque, Next Generation Photovoltaics: High Efficiency through Full Spectrum Utilization, Illustrated edition, CRC Press, 2010.
7. Ana BelénCristóbalLópez, Antonio Martí Vega, Antonio LuqueLópez, Next Generation of Photovoltaics: New Concepts, Illustrated edition, Springer, 2012.
8. M. A. Green, Third Generation Photovoltaics: Advanced Solar Energy Conversion, Springer, 2006.

COs:

The students will be able to:

1	Understand the basics solar irradiance.
2	Learn the basic operation principle of an ideal solar cell and its characteristics study.
3	Analyze the manufacturing process of crystalline silicon solar cell and its performance.
4	Learn about thin film technology solar cells and analyze its performance.

5 Apply the fundamentals of solar cells for the development of emerging thin film solar cells.

EC-5262	Reconfigurable hardware Design	L T P C
	M.Tech. (MVD), Second Semester (Elective – IV)	3 0 0 3

FPGA Architectures, CAD for FPGAs: Overview, LUT Mapping, Timing Analysis, P&R
Reconfigurable Devices: From Fine-grained to Coarse-Grained Devices
Reconfiguration Modes: Multi-context devices, Dynamic and Partial runtime Reconfiguration
Compilation from High Level Languages
System level design for reconfigurable computing: Heuristic Temporal Partitioning and ILP-based Temporal Partitioning, Behavioral Synthesis, Reconfigurable example systems' tool chains

Texts/References

1. Fine- and Coarse-grain Reconfigurable Computing, Dimitrios Soudris (editor) StamatisVassiliadis (editor), Springer Verlag, 2007
2. Dynamic Reconfiguration: Architectures and Algorithms, Jerry L. Trahan Ramachandran Vaidyanathan, Plenum Pub Corp, December 1, 2003
3. http://www.cse.iitd.ernet.in/~kolin/Courses/2006

COs:
The students will be able to:

1. Learn architectural behavior of FPGA.
2. Analyze Look up table (LUT) based design.
3. Investigate the timing analysis of various circuits
4. Perform partitioning, behavioral synthesis, runtime configuration schemes.
5. Implement reconfigurable design using FPGA for various applications.

EC-5263	Advanced CMOS Devices And Technology	L T P C
	M.Tech. (MVD), Second Semester (Elective – III)	3 0 0 3

Fundamentals

History of Si technology, Review of CMOS scaling. Problems with traditional geometric scaling. Power crisis. Review of basic quantum mechanics. Mobility enhancement techniques. Review of stress and strain, how it affects band structure of silicon. Types and realization of stress elements. Problems with stress elements.

High-K Gate Dielectric and process

Gate oxide scaling trend. Urgency to switch gate dielectric material. High K material selection. Fermi level pinning Process integration of high K gate dielectrics and metal gates Multi-gate transistors. Ways of realization. Fabrication issues and integration challenges.

SOI Devices

Basic principle of MOSFETs, Introduction to classical planer bulk MOSFETs, VMOS devices. Introduction to SOI Technology, radiation hardness capability. Partially depleted SOI MOSFET, Fully depleted SOI MOSFET. Single gate SOI MOSFET, Double Gate SOI MOSFET, kink effect, Floating Body effect, Applications of SOI MOSFET, Comparison with Classical planer bulk MOSFET.

Multigate CMOS devices

Introduction to Finfets, Ways of realization, Fabrication issues and integration challenges.

CMOS compatible memory devices

Analog and digital benchmarking of models. Layout dependent effects. Test structures used for characterization, Variations and how it can affect scaling. Basics of sub wavelength lithography. Design for manufacturability.

References:

1. Hei Wong, "Nano-CMOS Gate Dielectric Engineering," CRC, 2011.
2. J.P. Colinge, "FinFETs and Other Multi-Gate Transistors," Springer, 2010.
3. B. Wong, A. Mittal, Y. Cao, G. Starr, "Nano-CMOS Circuit and Physical Design", Wiley Inter-science 2004.
4. A. Dimoulas, E. Gusev, P. McIntyre, M. Heyns, "Advanced Gate Stacks for High-Mobility Semiconductors", Springer 2007.

COs:

The students will be able to

1. Understand the scaling rules, power crisis.
2. Analyze the impact of gate oxide scaling issues of the devices
3. Demonstrate the SOI device Technology considering fully depleted and partially depleted case
4. Illustrate the multigate device physics
5. Apply the concept of benchmarking analog and digital models and layouting

EC-5264	Flexible Electronics	L T P C
	M.Tech. (MVD), Second Semester (Elective – IV)	3 0 0 3

Flexible Electronics Basics: Introduction to Flexible and Printed Electronics and their Materials Systems, Background and history, emerging technologies, general applications, Review of Semiconductors and Circuit Elements, Carrier transport, doping, band structure, thin-film electronic devices.

Flexible Devices Fabrication and Materials: Thin-film Deposition and Processing Methods for Flexible Devices, CVD, ECVD, PVD, etching, photolithography, low-temperature process integration, Materials

for Flexible and Printed Electronics: Nanowire and nanoparticle synthesis, transition metal oxides, amorphous thin films, polymeric semiconductors, paper-based electronics, textile substrates, barrier materials.

Thin Film Transistors: Thin Film Transistors device structure and performance: I-V characteristics, Mechanics of Thinfilms and Flexible Thin-film Transistors: thin-film mechanics models, neutral plane, conformal electronics, mechanical modelling.

Patterning Process, Interfaces: Solution-based Patterning Processes: Ink-jet printing, gravure, imprint lithography, spray pyrolysis, surface energy effects, multilayer patterning Contacts and Interfaces to Organic and Inorganic Electronic Devices: Schottky contacts, defects, carrier recombination, effect of applied mechanical strain.

Applications and Economics: Flexible Electronics Applications: Displays, sensor arrays, memory devices, MEMS, lab-on-a chip, and photovoltaics, Introduction to Cost Models and Economics of Printed Flexible Electronics: Overview of display industry cost models, cost advantages and disadvantages for printed electronics, scaling of large-area flexible systems, cost of goods sold for display applications.

References:

1. Wong, William S., Salleo, Alberto (Editors) – Flexible Electronics: Materials and Application

Springer,U.S./India – 2009 – ISBN: 9781441944948 – DOI: 10.1007/978-0-387-74363-9

2. Guozhen Shen, Zhiyong Fan (Editor) - Flexible Electronics: From Materials to Devices – World

Scientific, U.S. –2016 – ISBN: 9789814651981

3. Takao Someya (Editor) – Stretchable Electronics – Wiley International, U.S. – 2013 – ISBN:

9783527329786

COs:

The students will be able to:

1 Select appropriate materials and manufacturing methods to design a process flow for fabricating flexible electronic device
2 Apply the fundamentals of electronic properties and role of interface in flexible and printed circuit systems
3 Explain the working principles of flexible devices like display, memory, photovoltaic cell, sensors, MEMS
4 Distinguish the electrical, mechanical properties of thin film transistor
5 Interpret the main challenges in materials and process selection, and circuit design for deformable circuitry.

EC-5265	Optimization Techniques in Engineering	L T P C
	M.Tech. (MVD), Second Semester (Elective – IV)	3 0 0 3

Introduction and Basic Concepts: Historical Development; Engineering applications of Optimization; Art of Modelling, Objective function; Constraints and Constraint surface; Formulation of design

problems as mathematical programming problems, Classification of optimization problems, Optimization techniques – classical and advanced techniques.

Optimization using Calculus: Stationary points; Functions of single and two variables; Global Optimum, Convexity and concavity of functions of one and two variables, Optimization of function of one variable and multiple variables; Gradient vectors; Examples, Optimization of function of multiple variables subject to equality constraints; Lagrangian function, Optimization of function of multiple variables subject to equality constraints; Hessian matrix formulation; Eigen values, Kuhn-Tucker Conditions; Examples.

Linear Programming: Standard form of linear programming (LP) problem; Canonical form of LP problem; Assumptions in LP Models; Elementary operations, Graphical method for two variable optimization problem; Examples, Motivation of simplex method, Simplex algorithm and construction of simplex tableau; Simplex criterion; Minimization versus maximization problems, Revised simplex method; Duality in LP; Primaldual relations; Dual Simplex method; Sensitivity or post optimality analysis, Other algorithms for solving LP problems – Karmarkar's projective scaling method.

Linear Programming Applications: Use of software for solving linear optimization problems using graphical and simplex methods, Examples for Communication, Networking, VLSI circuits, Devices, Antenna, MEMS etc.

Dynamic Programming: Sequential optimization; Representation of multistage decision process; Types of multistage decision problems; Concept of sub optimization and the principle of optimality, Recursive equations – Forward and backward recursions; Computational procedure in dynamic programming (DP), Discrete versus continuous dynamic programming; Multiple state variables; curse of dimensionality in DP.

Dynamic Programming Applications: Problem formulation and application in Design of continuous beam and Optimal geometric layout of a truss, Application in VLSI routing, Floor plan, device etc.

Advanced Topics in Optimization: Piecewise linear approximation of a nonlinear function, Multi objective optimization – Weighted and constrained methods; Multi level optimization, Evolutionary algorithms for optimization and search.

References:

1. An introduction to Optimization by Edwin P K Chong, Stainslaw Zak.
2. Nonlinear Programming by Dimitri Bertsekas.

COs:

The students will be able to:

1 Understand the applications of Optimization in various engineering fields
2 Apply different mathematical functions for optimization
3 Solve optimization problems using linear programming and dynamic programming
4 Implement various advanced optimization techniques for practical applications

Semester-III

EC-6298	Project Phase-I	L T P C
		0 0 0 6

COs:

The students will be able to:

CO1: Identify and formulate advanced research problems in Microelectronics and VLSI design areas through a comprehensive review of relevant literature.
CO2: Apply advanced concepts, mathematical models, and engineering principles to develop innovative solutions for complex Microelectronics and VLSI design problems.
CO3: Design, simulate, and implement advanced devices, VLSI circuits and systems using appropriate EDA tools, technologies, and methodologies.
CO4: Conduct systematic experiments, analyze and interpret results, validate proposed designs, and effectively communicate research findings through Patents, Journals and oral presentations in various conferences.

Semester-IV

EC-6299	Project Phase-II	L T P C
		0 0 0 6

COs:

The students will be able to:

CO1: Identify and formulate advanced research problems in Microelectronics and VLSI design areas through a comprehensive review of relevant literature.
CO2: Apply advanced concepts, mathematical models, and engineering principles to develop innovative solutions for complex Microelectronics and VLSI design problems.
CO3: Design, simulate, and implement advanced devices, VLSI circuits and systems using appropriate EDA tools, technologies, and methodologies.
CO4: Conduct systematic experiments, analyze and interpret results, validate proposed designs, and effectively communicate research findings through Patents, Journals and oral presentations in various conferences.