EC-5255 System on Chip

 L T P C M.Tech. (MVD), Second Semester (Elective – IV)

3 0 0 3

Design of System on a Chip: Introduction, Moore’s Law and the consequences, The International roadmap for semiconductor technology, the technology, and the tide of the markets

BJT Modeling with VBIC: Introduction, VBIC equivalent network, VBIC model formulation, parameter extraction, relationship between SGP and VBIC parameters, VBIC dc modeling, electro-thermal examples, high frequency modelling

 A MOS Transistor Model for Mixed Analog-digital Circuit Design and Simulation: Introduction, the long-channel model, the static model for short and narrow geometries, the charge and thermal noise models

Model Application And Experimental Results: The computer simulation model, Hierarchical model structure, Statistical circuit simulation including matching, The pinch-off voltage measurement and parameter extraction method, Parameter extraction sequence

Efficient Statistical Modeling for Circuit Simulation: introduction, classification of statistical models, hierarchy of statistical variations, process and geometry level modeling, existing statistical modeling approaches, SPICE model parameter perturbation, typical case modeling, distributional statistical modeling, specific case statistical modeling, generic case statistical modeling

Retargetable Application-driven Analog-digital Block Design: Introduction, analog-digital interface requirements, design flow and CAD support, retargetable block design, examples from industry practice

Robust Low Voltage Low Power Analog MOS VLSI Design: Introduction, low voltage CMOS squarelaw composite cells, statistical VLSI design tools and techniques, statistical design of the CMOS square law CMOS cells

Ultralow-Voltage Memory Circuits: Introduction, design issues for ultralow-voltage RAMs, DRAM circuits, ultralow-voltage SRAM circuits, perspectives, SOI CMOS technology

Low-voltage Low-power High-speed I/O Buffers: Introduction, various types of buffers: CMOS, HSTL, (High-Speed Transistor Logic), GTL/NTL (Gunning Transistor Logic / NMOS Transistor Logic), PCML (Pseudo Current Mode Logic), PECL (Pseudo Emitter Coupled Logic), USB (Universal Serial Bus), Matched-Impedance Buffer, Hyper-LVDS’ (Low-Voltage Differential-Signals)

Texts/References

1. Design Of System On A Chip: Devices and Components, Jochen Jess (editor), Ricardo A. L. Reis (editor) Ricardo A. L. Reis, Kluwer Academic Pub, 2004

2. Design of System on a Chip By: Ricardo Reis, Jochen Jess (Eds.), Springer-Verlag, 2004

3. ARM System-on-Chip Architecture (2nd Edition)by Stephen B. Furber, Steve B. Furber, Addison Wesley, Aug. 2000, ISBN: 0201675196.

4. Real-Time Concepts for Embedded Systems, by Qing Li, Caroline Yao, CMP Books, July 2003, ISBN: 157820124.

5. Fundamentals of Embedded Software: Where C and Assembly Meet, by Daniel Wesley Lewis, Prentice Hall, Nov. 2001. 21

COs:

The students will be able to:

C1.Explain the importance of an efficient system-on-chip communication infrastructure

C2.Gain idea and knowledge about statistical models, SPICE, SRAM

C3.Able to design ultra-low voltage memory circuits.

C4.Gain knowledge about low voltage, low power I/O buffers.

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| No of Lectures | Topic | CO |
| 1,2.3 | Design of System on a Chip: Introduction, Moore’s Law and the consequences,  | CO1 |
| 4,5.6 | The International roadmap for semiconductor technology, and the tide of the markets | CO1 |
| 7,8,9 | BJT modelling with VBIC,relationship between SGP and VBIC parameters, VBIC dc modeling, electro-thermal examples, high frequency modelling | CO1 |
| 10,11,12 | A MOS Transistor Model for Mixed Analog-digital Circuit Design and Simulation:  | CO1 |
| 13,14,15 | Introduction, the long-channel model, the static model for short and narrow geometries, the charge and thermal noise models | CO1 |
| 16,17,18 | Model Application And Experimental Results: The computer simulation model, Hierarchical model structure, Statistical circuit simulation including matching, The pinch-off voltage measurement and parameter extraction method, Parameter extraction sequence  | CO2 |
| 19,20,21 | Efficient Statistical Modeling for Circuit Simulation: introduction, classification of statistical models, hierarchy of statistical variations, process and geometry level modeling, existing statistical modeling approaches, SPICE model parameter perturbation, typical case modeling, distributional statistical modeling, specific case statistical modeling, generic case statistical modeling  | CO2 |
| 22,23,24,25,26 | Retargetable Application-driven Analog-digital Block Design: Introduction, analog-digital interface requirements, design flow and CAD support, retargetable block design, examples from industry practice  | CO2 |
| 27,28,29 | Robust Low Voltage Low Power Analog MOS VLSI Design: Introduction, low voltage CMOS squarelaw composite cells, statistical VLSI design tools and techniques, statistical design of the CMOS square law CMOS cells  | CO3 |
| 30,31,32,33 | Ultralow-Voltage Memory Circuits: Introduction, design issues for ultralow-voltage RAMs, DRAM circuits, ultralow-voltage SRAM circuits, perspectives, SOI CMOS technology  | CO3 |
| 34 to 40 | Low-voltage Low-power High-speed I/O Buffers: Introduction, various types of buffers: CMOS, HSTL, (High-Speed Transistor Logic), GTL/NTL (Gunning Transistor Logic / NMOS Transistor Logic), PCML (Pseudo Current Mode Logic), PECL (Pseudo Emitter Coupled Logic), USB (Universal Serial Bus), Matched-Impedance Buffer, Hyper-LVDS’ (Low-Voltage Differential-Signals) | CO4 |