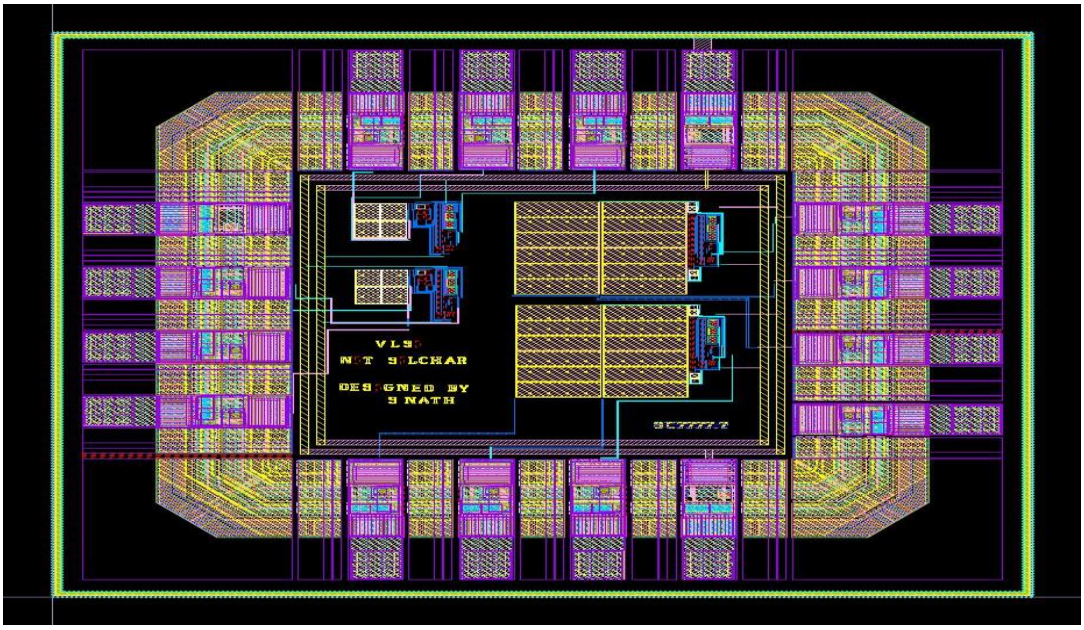
Dear Sir/ Madam

It is our pleasure to share that VLSI Lab of Electronics and Communication Engineering has accomplished its 1st VLSI chip tape out made by indigenous using the SCL Mahali foundry, 180 nm Technology node. Presently VLSI Lab is working on a few more tape-out using TSMC Foundry in 65 nm Technology node.

In electronics design, **Tapeout** is the final result of the design process for integrated circuits or printed circuit boards before they are sent for manufacturing. The Tapeout is specifically the point at which the graphic for the photomask of the circuit is sent to the fabrication facility.



With the completion 1st tape-out, Electronics and Communication is one step ahead in VLSI design and claiming one of the premier Centre for VLSI Design in India. Department is expecting a few more patents from the final chips and also looking for commercial licensing of our physical products in near future.

Thanks to all the members of VLSI design group of ECE Dept. Special Thanks to our backend design Engineer **Mr sourav Nath** for his hard working and dedications. Without his unabated effort, ECE Dept could not achieve this milestone. Thanks to IISC Bangalore for giving awesome hands-on-Training of Chip design under SMDP C2SD project. Thanks to MeitY and authority of NIT Silchar for all the way support to meet the target.

We invite interested students/ faculty members to join hands with our group for collaborative work in future.

Dr K L Baishnab

Chief Investigator of SMDP- C2SD project, MeitY

Dr Koushik Guha

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